UNITED STATES PATENT APPLICATION

of

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for

TEMPERATURE AND JITTER COMPENSATION CONTROLLER CIRCUIT AND METHOD FOR FIBER OPTICS DEVICE

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TEMPERATURE AND JITTER COMPENSATION CONTROLLER CIRCUIT AND METHOD FOR FIBER OPTICS DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claim priority to and benefit of U.S. Provisional Patent Application No. 60/425,001, filed November 8, 2002 and entitled "Temperature and Jitter Compensation Controller Circuit and Method for Fiber Optics Transceiver," which application is incorporated herein by reference in its entirety.

[0002] This application is also related to co-pending U.S. Provisional Patent Application No. 60/425,003, filed November 8, 2002, which application is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. The Field of the Invention

[0003] The present invention relates generally to the field of optoelectronic devices. More particularly, the invention relates to systems and methods for controlling operating requirements of an optoelectronic device at various operating temperatures.

2. The Relevant Technology

[0004] Figure 1 shows a schematic representation of the essential features of a typical conventional fiber optic transceiver. The main circuit 1 contains at a minimum transmit and receive circuit paths and power 19 and ground connections 20. The receiver circuit typically consists of a Receiver Optical Subassembly (ROSA) 2 which contains a mechanical fiber receptacle and coupling optics as well as a photodiode and pre-amplifier (preamp) circuit. The ROSA is in turn connected to a post-amplifier (postamp) integrated circuit 4, the function of which is to generate a fixed output swing digital signal which is connected to outside circuitry via the RX+ and RX- pins 17. The

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postamp circuit 4 also often provides a digital output signal known as Signal Detect or Loss of Signal indicating the presence or absence of suitably strong optical input. The Signal Detect output is provided at output pin 18.

[0005] The transmit circuit will typically consist of a Transmitter Optical Subassembly (TOSA) 3 and a laser driver integrated circuit 5. The TOSA contains a mechanical fiber receptacle and coupling optics as well as a laser diode or LED. The laser driver circuit 5 will typically provide AC drive and DC bias current to the laser. The signal inputs for the AC driver are obtained from the TX+ and TX- pins 12. The laser driver circuitry typically will require individual factory setup of certain parameters such as the bias current (or output power) level and AC modulation drive to the laser. Typically this is accomplished by adjusting variable resistors or placing factory selected resistors 7, 9 (i.e., having factory selected resistance values). Additionally, temperature compensation of the bias current and modulation is often required. This function can be integrated in the laser driver integrated circuit or accomplished through the use of external temperature sensitive elements such as thermistors 6, 8.

[0006] In addition to the most basic functions described above, some optoelectronic device platform standards involve additional functionality. Examples of this are the TX disable 13 and TX fault 14 pins described in the Gigabit Interface Converter (GBIC) standard. In the GBIC standard (SFF-8053), the TX disable pin 13 allows the transmitter to be shut off by the host device, while the TX fault pin 14 is an indicator to the host device of some fault condition existing in the laser or associated laser driver circuit.

[0007] In addition, the GBIC standard includes a series of timing diagrams describing how these controls function and interact with each other to implement reset

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operations and other actions. Most of this functionality is aimed at preventing non-eyesafe emission levels when a fault condition exists in the laser circuit. These functions may be integrated into the laser driver circuit 5 itself or in an optional additional integrated circuit 11.

[0008] Finally, the GBIC standard for a Module Definition "4" GBIC also requires the EEPROM 10 to store standardized ID information that can be read out via a serial interface (defined as using the serial interface of the ATMEL AT24CO1A family of EEPROM products) consisting of a clock 15 and data line 16.

[0009] As an alternative to mechanical fiber receptacles, some conventional optoelectronic devices use fiber optic pigtails which are unconnectorized fibers.

[0010] Similar principles apply to fiber optic transmitters or receivers.

[0011] In order to maximize the performance and product life of an optoelectronic device, it is advantageous to configure the operating parameters of the optoelectronic device so as to perform temperature compensation and minimize jitter over a range of temperatures at a desired "extinction ratio" and optical power level.

[0012] One conventional approach uses a fixed set of temperature compensation parameters for all optoelectronic devices whose components and configurations are otherwise identical. Under high-volume manufacturing conditions, however, this approach is not desirable because the performance and behavior of the components comprising an optoelectronic device vary from component to component. Therefore, the use of universal temperature compensation parameters has different temperature and jitter compensation effects on different modules within a class of similarly configured optoelectronic devices, thereby not achieving the desired efficiency for individual optoelectronic devices.

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[0013] Another approach uses a temperature controller to maintain a steady operating temperature for the optoelectronic device. This approach, however, is generally not feasible for pluggable optoelectronic devices because temperature controllers are typically too big to fit within such devices. For example, the dimensions for a pluggable optoelectronic device specified by GBIC standards are 1.2" x 0.47" x 2.6", and the dimensions for an optoelectronic device specified by SFP (Small Form Factor Pluggable) standards are 0.53" x 0.37" x 2.24". As pluggable optoelectronic devices become more and more compact, the use of a temperature controller in these devices is becoming less and less feasible. In addition, temperature controllers can be very expensive, thus increasing or rendering infeasible the cost of manufacturing the optoelectronic device.

[0014] Accordingly, what is needed is a control circuit for an optoelectronic device, and method to configure the circuit for each individual device so as to minimize jitter and improve the temperature performance for each individual optoelectronic device.

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SUMMARY OF THE INVENTION

[0015] The present invention provides systems and methods for implementing a controller in an optoelectronic device in order to control various operating requirements at different operating temperatures of an optoelectronic device. In one aspect of the invention, the optoelectronic device includes a controller integrated circuitry which includes memory for containing information regarding control parameters for various operating requirements. The optoelectronic device references and uses these control parameters to control operating requirements at various operating temperatures. Exemplary embodiments are described with reference to a transceiver, although it is understood that the systems and methods of the invention may extend to any optoelectronic device.

[0016] In one aspect of the invention, the control parameters are determined according to the following method. First, the optoelectronic transceiver is situated in a temperature control chamber. A test controller or host computer is coupled to the optoelectronic transceiver. An electrical test signal is provided to the transmitter-portion of the optoelectronic transceiver, while the signal transmitted from the optical portion of the optoelectronic transceiver is received by an optical signal analyzer which is coupled to the host computer.

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[0017] The optical power level and "extinction ratio" of the optoelectronic transceiver are set to a predetermined level corresponding to efficient operation of the optoelectronic transceiver. The temperature of the temperature control chamber is set to a first predetermined temperature, preferably room temperature, and a control parameter (e.g., AC bias, DC bias, and the like.) is adjusted to satisfy an operating requirement (e.g., jitter minimization). The temperature control chamber is set to at least a second

predetermined temperature, preferably near the upper end of the operating range of the optoelectronic transceiver, and the above process is repeated.

[0018] The adjusted control parameter values at the predefined temperatures are then used to calculate a table of interpolated control parameter values throughout a multitude of intermediate temperatures within the range of operating temperatures for the optoelectronic transceiver. These calculated control parameter values are then stored in the transceiver's memory to be accessed during operation of the transceiver when the transceiver reaches the specific predefined temperatures within the transceiver's temperature operating range.

[0019] In another aspect of the invention, multiple control parameters are adjusted to satisfy at least one operating requirement. In yet another aspect of the invention, multiple devices are tested simultaneously, the plurality of devices being evaluated at a first temperature before setting the temperature control chamber to another temperature.

[0020] These and other advantages and features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0021] To further clarify the above and other advantages and features of the present invention, a more particular description of the invention will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. It is appreciated that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope. The invention will be described and explained with additional specificity and detail through the use of the accompanying drawings, in which:

[0022] Figure 1 illustrates a block diagram of a prior art optoelectronic transceiver.

[0023] Figure 2 is a block diagram of an optoelectronic transceiver in accordance with an embodiment of the present invention.

[0024] Figure 3 is a block diagram of modules within the controller IC of the optoelectronic transceiver of Figure 2.

[0025] Figure 4 is a block diagram of a system for testing and configuring an optoelectronic transceiver in accordance with an embodiment of the present invention.

[0026] Figure 5 is a conceptual representation of temperature compensation as performed during operation of an optoelectronic transceiver in accordance with an embodiment of the present invention.

[0027] Figure 6 is a conceptual representation of the relationship of DC Bias Current to Optical Output Power at various temperatures for the optoelectronic transceiver of Figure 2.

[0028] Figure 7 is a block diagram of an avalanche photodiode and its support circuitry in accordance with an embodiment of the present invention.

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[0029] Figure 8 is a block diagram of a system for testing and configuring an avalanche photodiode in accordance with an embodiment of the present invention.

[0030] Figure 9 is a representation of an optical signal with jitter as seen by an optical signal analyzer.

[0031] Figure 10 is a flow-chart of a method for calibrating an optoelectronic transceiver in accordance with an embodiment of the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0032] Preferred embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described. It will be appreciated that in the development of any such embodiment, numerous implementation-specific decisions must be made to achieve the designers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure. Furthermore, while exemplary embodiments describe a transceiver, it is appreciated that the present invention extends to any optoelectronic device including, but not limited to, transceivers, transponders, transmitters and receivers.

[0033] An exemplary optoelectronic transceiver 100 incorporating features of the present invention is shown in Figures 2 and 3. The transceiver 100 contains a receiver circuit, a transmitter circuit, a power supply voltage 19 and ground connections 20. The receiver circuit of the transceiver includes a Receiver Optical Subassembly (ROSA) 102, which may contain a mechanical fiber receptacle as well as a photodiode and pre-amplifier (preamp) circuit. The ROSA 102 is in turn connected to a post-amplifier (postamp) integrated circuit 106, the function of which is to generate a fixed output swing digital signal which is connected to outside circuitry via the RX+ and RX- pins 17. The postamp circuit 106 also often provides a digital output signal known as Signal Detect or Loss of Signal indicating the presence or absence of suitably strong optical input. The postamp circuit 106 does not necessarily have to be used to generate

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the Signal Detect or Loss of signal. In alternative embodiments, the postamp circuit 106 could be replaced with a CDR **[what does this stand for?]** or a demux chip, which embodiments are not shown.

[0034] The transmit circuit of the transceiver includes a Transmitter Optical Subassembly (TOSA) 104 and a laser driver integrated circuit 108. The TOSA 104 contains a transmitter, generally a laser diode or LED, and may also include a mechanical fiber receptacle. As an alternative to mechanical fiber receptacles, some transceivers use fiber optic pigtails, which are standard, male fiber optic connectors. A laser driver circuit 108 provides AC drive and DC bias current to the laser diode or LED in the TOSA 104. The signal inputs for the laser driver 108 are obtained from the TX+ and TX- pins 12.

[0035] In addition to the basic functions described above, some transceiver platform standards involve additional functionality. Examples of this are the transmitter disable (TX disable) pin 13 and transmitter fault (TX fault) pin 14 described in the GBIC standard, as well as other optoelectronic transceiver standards. In these transceiver standards, the TX disable pin 13 allows the transmitter to be shut off by the host device, while the TX fault pin 14 is an indicator to the host device of some fault condition existing in the laser or associated laser driver circuit. In addition, these standards define how these controls function and interact with each other to implement reset operations and other actions.

[0036] Some of this functionality is aimed at preventing non-eyesafe emission levels when a fault condition exists in the laser circuit. These functions may be integrated into the laser driver circuit 108 itself or in a controller integrated circuit 110. Finally, many of the optoelectronic transceiver standards also require that a memory

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device in the transceiver 100 store standardized serial ID information that can be read out via a serial interface (defined as using the serial interface of the ATMEL AT24C01A family of EEPROM products) having a clock line (SCL) 15 and a data line (SDA)16.

[0037] Control and setup functions of the transceiver 100 are implemented with the controller IC 110, which in one embodiment is implemented as a single-chip integrated circuit. The controller IC 110 handles all low speed communications with a host device. These include the standardized pin functions such as Loss of Signal (LOS) 11, TX fault pin 14, and the TX disable pin 13.

[0038] All the components of the transceiver 100 are preferably located in a protective housing except for connectors that may protrude from the housing. Suitable housings, including metallic, plastic, potting box and other housing structures are well known in the art.

[0039] With reference to Figure 3, the controller IC 110 is shown in further detail. Controller IC 110 has a two-wire serial interface 121, also called the memory interface, for reading and writing to memory mapped locations in the controller IC. The interface 121 is coupled to host device interface input/output lines, typically clock (SCL) and data (SDA) lines, 15 and 16. In one embodiment, the serial interface 121 operates in accordance with the two wire serial interface standard that is also used in the GBIC and SFP standards. Other interfaces could be used in alternate embodiments.

[0040] The two wire serial interface 121 is used for all setup and querying of the controller IC 110, and enables access to the optoelectronic transceiver's control circuitry as a memory mapped device. That is, tables and parameters are set up by writing values to predefined memory locations of one or more memory devices 120, 122, 128 (e.g.,

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EEPROM devices) in the controller, whereas diagnostic and other output and status values are output by reading predetermined memory locations of the same memory devices 120, 122, 128. At least some of these memory devices are nonvolatile memory devices that retain the values stored in them even when electrical power is not provided to the transceiver 100. The serial interface 121 is consistent with currently defined serial ID functionality of many transceivers where a two wire serial interface is used to read out identification and capability data stored in an EEPROM. As shown in Figure 3, the controller IC 110 includes a General Purpose EEPROM 120, a temperature lookup table 122, and a diagnostic value and flag storage 128.

[0041] It is noted here that some of the memory locations in the memory devices 120, 122, 128 are dual ported, or even triple ported in some instances. That is, while these memory mapped locations can be read and in some cases written via the serial interface 121, they are also directly accessed by other circuitry components in the controller IC 110. For instance, certain "margining" values stored in memory 120 are read and used directly by logic 134 to adjust (i.e., scale upwards or downwards) drive level signals being sent to the digital to analog output devices 123. Similarly, there are flags stored in memory 128 that are (A) written by logic circuit 131, and (B) read directly by logic circuit 133. An example of a memory mapped location not in the memory devices but that is effectively dual ported is the output or result register of clock 132. In this case the accumulated time value in the register is readable via the serial interface 121, but is written by circuitry in the clock circuit 132.

[0042] In addition to the result register of the clock 132, other memory mapped locations in the controller IC 110 may be implemented as registers at the input or output of respective sub-circuits of the controller. For instance, the margining values used to

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control the operation of logic 134 may be stored in registers in or near logic 134 instead of being stored within memory device 128.

[0043] As shown in Figures 2 and 3, the controller IC 110 has connections to the laser driver 108 and receiver components. These connections serve multiple functions. The controller IC 110 has a multiplicity of digital to analog converters 123. In one embodiment the digital to analog converters are implemented as current sources, but in other embodiments the digital to analog converters may be implemented using voltage sources. In yet other embodiments, the digital to analog converters may be implemented using digital potentiometers. In some embodiments, the output signals of the digital to analog converters are used to control key parameters of the laser driver circuit 108. In particular, outputs of the digital to analog converters 123 are used to control the DC bias current as well as the AC modulation level of the electrical signal applied by the laser driver circuit 108 to the laser or LED in TOSA 104.

[0044] In some embodiments, the controller IC 110 includes mechanisms to compensate for temperature dependent characteristics of the laser in TOSA 104. This is implemented in the controller IC 110 through the use of temperature lookup tables 122 that are used to assign values to the control outputs of the controller IC 110 as a function of the temperature measured by a temperature sensor 125 within the controller IC 110 and/or the temperature measured by a temperature sensor in or near the TOSA 104. The controller IC 110 also receives a temperature input signal from a temperature sensor 125. The temperature sensor may be incorporated into the controller IC 110 or may be a separate device within the transceiver housing.

[0045] In particular, a current temperature value is obtained from a temperature sensor either in the controller IC 110 (e.g., sensor 125) or in or near the TOSA 104.

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That temperature value is converted into a digital value (by analog to digital converter (ADC) 127), and rounded or otherwise processed if necessary to form an index value for indexing into the temperature lookup tables 122. The index value is then used to lookup or access control parameter (e.g., AC bias, DC bias and APD bias) settings in the memory 122 (temperature lookup tables) corresponding to the current temperature in the transceiver. These control parameter settings are converted into analog signals by a set of digital to analog converters 123, and the resulting analog signals are used to control the operation of the laser driver 108, which, in turn, controls the laser diode or LED in the TOSA 104.

[0046] In one embodiment, the outputs of digital to analog converters 123 are current signals. In other embodiments, the controller IC 110 may use digital to analog converters with voltage source outputs or may even replace one or more of the digital to analog converters 123 with digital potentiometers to control the characteristics of the laser driver 108 in accordance with the control parameter settings obtained from the lookup tables in memory 122. It should also be noted that while Figure 2 shows a system where the laser driver 108 is specifically designed to accept inputs from the controller IC 110, it is possible to use the controller IC 110 with many other laser drivers to control their output characteristics.

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[0047] Figure 2 shows a number of connections to and from the laser driver 108 and the controller IC 110. In addition, controller IC 110 has connections to and from the ROSA 102 and Postamp 106. These are analog monitoring connections that the controller IC 110 uses to provide diagnostic feedback to the host device via memory mapped locations in the controller IC 110.

[0048] With reference to Figure 3, in one embodiment, the controller IC 110 has a multiplicity of analog inputs. The analog input signals indicate operating conditions of the transceiver and/or receiver circuitry. These analog signals are scanned by a multiplexer ("mux") 124 and converted using an analog to digital converter ("ADC") 127. In one embodiment, the ADC 127 has 12 bit resolution; although ADC's with other resolution levels may be used. The converted values are stored in predefined memory locations, for instance in the diagnostic value and flag storage device 128 shown in Figure 3, and are accessible to the host device via memory reads. These values are calibrated to standard units (such as millivolts or microwatts) as part of a factory calibration procedure.

[0049] Figure 4 is a block diagram of a system for testing and configuring an optoelectronic transceiver. The optoelectronic transceiver testing and configuration system 400 includes an optoelectronic transceiver 100 situated in an oven or temperature control chamber 402. In another embodiment, the optoelectronic transceiver 100 may be associated with a thermoelectric cooler which can be configured to increase or decrease the temperature of the optoelectronic device. A test controller or host computer 404 is coupled to the optoelectronic transceiver 100. Similarly, multiple optoelectronic transceivers 100 may be simultaneously tested and configured by adjusting the described connections and set-up to accommodate multiple transceivers.

[0050] A test signal is provided to the receiver portion of the optoelectronic transceiver through an optical fiber (RX) 408, while the signal transmitted from the optoelectronic transceiver through optical fiber (TX) 410 is received by an optical signal analyzer 406 (e.g., a digital communication analyzer) which is coupled to the host computer 404.

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[0051] The host computer 404 preferably contains a user interface 460, one or more interfaces (not shown) for connection to the temperature control chamber, a central processing unit ("CPU") 450 and a memory 470. The memory 470 may include high speed random access memory and may also include nonvolatile mass storage, such as one or more magnetic disk storage devices. The memory may include mass storage that is remotely located from the central processing unit(s).

[0052] The memory 470 preferably stores an operating system 472, control parameter setup procedures 474, operational requirement settings (e.g., jitter minimization) and temperature compensation values 476. The memory 470 may also include "extinction ratio" and optical power level setup procedures. The operating system 472 stores instructions for communicating, processing data, accessing data, storing data, searching data, etc. The control parameter setup procedures 474 are a set of instructions that test and configure the transceiver 100, described with respect to Figure 10. Temperature compensation values are recorded in the memory for use in computing temperature compensation and jitter minimization values at predefined temperatures, (see Figure 10).

[0053] The host computer 404 controls the function of the temperature control chamber 402 and the transceiver 100 being tested and configured. The host computer 404 is coupled to the transceiver 100 via a data bus 412, for transmitting and receiving test data patterns, and a control bus 414 that transmits control parameters (including computed temperature compensation values to be stored in the transceiver's 100 temperature look-up tables 122) from the host computer 404 to the transceiver 100, and transmits monitoring data from the transceiver 100 to the host computer 404.

[0054] The host computer 404 processes and records the settings and measurements made during the optoelectronic transceiver testing and configuration process. These settings and measurements preferably include the optical power level, "extinction ratio," jitter, temperature, APD bias level and DC and AC bias levels.

[0055] The optical signal analyzer 406 receives the optical test output signal via optical fiber (TX) 410 from the transceiver 100 and analyzes the test signal for compliance with pre-programmed operating requirements such as jitter minimization. The optical signal analyzer 406 is coupled to the host computer 404 and transmits the results of its analysis to the host computer 404 for further adjustment of the control parameters if necessary.

[0056] In another embodiment, analysis of the test signal for compliance with operating requirements can be done manually by viewing a scope, such as a digital communication analyzer ("DCA"), that displays the test signal. Necessary adjustments to control parameters are then communicated to the host computer 404 by the viewer until operating requirement compliance is achieved. In embodiments where there are multiple transceivers 100 in the temperature control chamber 402, the host computer 404 is selectively coupled to each of the transceivers 100 in the temperature control chamber 402 while the chamber is held at each calibration temperature, enabling the host computer 404 to test and calibrate each of the transceivers at that calibration temperature.

[0057] Figure 5 is a conceptual representation of the temperature compensation function of the controller IC 110 during operation of an optoelectronic transceiver 100. As the temperature changes during the operation of the optoelectronic transceiver 100, the temperature sensor 125 (see Figure 3) senses the temperature change and the

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corresponding control parameter values are sent from the temperature lookup table 122 (see Figure 3) to the interface 504. The control parameters preferably include the AC amplitude and the DC bias, and may include the APD (avalanche photo diode) bias, which is a voltage.

[0058] The interface 504 sends the appropriate digital AC amplitude value to a DAC (digital to analog converter) 506 and the resulting analog signal is conveyed, along with the data signal 508, to an amplifier 510. The data signal, as amplified by the amplifier 510 is sent to the TOSA 104.

[0059] Similarly, the interface 504 sends the appropriate digital DC bias value to a DAC 512 and the resulting analog signal is scaled at some predetermined ratio by a current mirror 514 before it is provided to the TOSA 104. This DC bias signal controls the average optical power (see Figure 6) output by the TOSA 104. In addition to performing a scaling function, the current mirror 514 performs an isolating function to prevent interference with the components and processes located elsewhere in the operational set-up explained above.

[0060] The interface 504 also sends the appropriate digital APD bias voltage value to a DAC 516 and the resulting analog signal is sent as a voltage source V_{APD} to the avalanche photodiode 704 shown in Figure 7.

[0061] Figure 6 is a conceptual representation of the relationship of DC Bias Current to Optical Output Power at various temperatures for the optoelectronic transceiver 100. The lines, Tl, T2 and T3, represent the optical output power at various temperatures as a function of the DC bias. The point where the desired average optical power P_{ave} intersects with the temperature lines Tl, T2 and T3 is the preferred DC bias setting Bias A, Bias B and Bias C, respectively. Interpolation is used to calculate the

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preferred DC bias settings, or control parameters, at predetermined temperatures between the temperatures Tl, T2 and T3 with known preferred DC bias values.

[0062] Figure 7 is a block diagram of one embodiment of an avalanche photodiode and its support circuitry. These components are all located within the transceiver housing. A reverse-bias voltage V_{APD} originating from the temperature lookup table 122 and based on the relevant temperature is applied to an avalanche photodiode 704.

[0063] As is well known in the art, if the reverse-bias voltage applied to an avalanche photodiode is increased, an avalanche breakdown will eventually occur at a characteristic avalanche voltage V_A. The avalanche voltage V_A is typically in a range between 40 volts and 70 volts at room temperature; however it varies from one device to another and also varies as a (generally increasing) function of the temperature of the avalanche photodiode. The sensitivity of an avalanche photodiode is maximized when it is operated at a reverse-bias voltage V_{APD} that is less than the avalanche voltage V_A by an offset voltage that is relatively small (approximately 1 volt for some avalanche photodiodes). It is in this way that the controller IC 110 in conjunction with the values stored in the temperature lookup tables 122 are used to regulate the reverse-bias voltage V_{APD} applied to an avalanche photodiode so that the maximum sensitivity of the avalanche photo diode is maintained over a range of temperatures.

[0064] The output signal from the avalanche photo diode 704 is amplified by a transimpedance amplifier (TIA) 702 and then amplified by a post-amplifier (postamp) integrated circuit 106, a CDR(not shown) or a demux chip (not shown). The postamp 106 generates a fixed output swing digital signal which is connected to outside circuitry via the RX+ and RX- pins 17.

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[0065] Figure 8 is a block diagram of a system for testing and configuring an avalanche photodiode ("APD"). The APD testing and configuration system 800, which is the test set-up for working with the APD control components 700 set-up shown in Figure 7, includes an optoelectronic transceiver 100 situated in an oven or temperature control chamber 402. A test controller or host computer 404 is coupled to the optoelectronic transceiver 100. The host computer 404 and its connections to the temperature control chamber 402 and transceiver 100 are described above with reference to Figure 4.

[0066] An optical signal is preferably applied to the transceiver 100 in order to perform tests and configurations based on application and related assumptions. A ROSA test data stream source 802 feeds a test signal to the receiver portion of the optoelectronic transceiver 100 through an optical fiber (RX) 408. In an optional configuration, the signal transmitted from the optoelectronic transceiver 100 through optical fiber (TX) 410 is received by the ROSA test data stream source 802.

[0067] Figure 9 is a representation of an optical signal with jitter as seen by an optical signal analyzer. The minimization of jitter improves signal clarity and intensity. Jitter is the width of the "50% line" as represented in Figure 9. The control parameters are adjusted during the testing and configuration phase of the optoelectronic transceiver 100 to reduce the jitter width, thereby improving the quality of the outgoing signal.

[0068] Figure 10 is a flow-chart of a method for calibrating an optoelectronic transceiver 100. The optical power level and "extinction ratio" of the optoelectronic transceiver 100 are set to a predetermined level corresponding to efficient operation of the optoelectronic transceiver and the specifications in the data sheet. Once the transceiver 100 is placed in the temperature control chamber 402, or similar temperature

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controlled environment, at step 1002, the temperature control chamber 402 is set to a first temperature at one end of the temperature calibration range, preferably room temperature. The temperature calibration range is preferably similar to or greater than the operating range of the optoelectronic transceiver 100. At step 1004, the temperature control chamber 402 is stabilized at the first temperature.

[0069] At step 1006, the desired control parameters (e.g., AC bias, DC bias, etc.) are set at the first temperature to satisfy an operating requirement (e.g., jitter minimization). Alternatively, multiple control parameters can be adjusted to satisfy multiple operation requirements at the first temperature. At step 1008, the values of the control parameters are recorded at an entry (e.g., in a table in memory) for the first temperature for use in later calculations.

[0070] At step 1010, the temperature control chamber 402 is then set to at least a second temperature within the temperature calibration range. If calibration is being performed at just two temperatures, the second temperature is preferably near the upper end of the operating range of the optoelectronic transceiver 100; otherwise the second temperature is preferably a second temperature in a predefined sequence of calibration temperatures. At step 1012, the temperature control chamber 402 is stabilized at this second temperature. At step 1014, the control parameters are adjusted as necessary to satisfy one or more operating requirements. At step 1016, the values of the control parameters are then recorded in the memory of the host computer 404 for use in later calculations. The process of setting a predetermined temperature, adjusting one or more control parameters to meet one or more operating requirements, and storing the results may be repeated at multiple calibration temperatures.

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[0071] At step 1018, the recorded control parameter values at the predefined temperatures are then used to calculate (e.g., using linear interpolation) a table of interpolated control parameter values corresponding to each operating requirement throughout a multitude of predefined intermediate temperatures within the range of operating temperatures for the optoelectronic transceiver 100. At step 1020, these control parameter tables are then stored in the temperature look-up tables 122 of the transceiver 100 to be accessed during operation of the transceiver when it reaches the specific predefined temperatures within the transceiver's temperature operating range.

[0072] In embodiments in which multiple transceivers are tested and calibrated simultaneously, certain steps of the procedures represented by Figure 10 are repeated for each respective transceiver in the test chamber. In particular, steps 1006, 1008, 1014 and 1016 are each repeated for every respective transceiver in the test chamber before the calibration procedure moves onto the next step. Similarly, interpolation and storage steps 1018 and 1020 are performed for each respective transceiver.

[0073] Examples of operating requirements that are effected by control parameters include jitter minimization, optical output power, extinction ratio, crossing percentage, mask hits, mask margin, avalanche photodiode temperature compensation, and the like.

[0074] Some aspects of the present invention can be implemented as a computer program product that includes a computer program mechanism embedded in a computer readable storage medium. For instance, the computer program product could contain the program modules for embodiments discussed regarding Figures 4, 8 and 10. These program modules may be stored on a CD-ROM, magnetic disk storage product, or any other computer readable data or program storage product. The software modules in the

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computer program product may also be distributed electronically, via the Internet or otherwise, by transmission of a computer data signal (in which the software modules are embedded) on a carrier wave.

[0075] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

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